A Review of High-Impedance and Low-Impedance Differential Relaying for Bus Protection

Suparat Pavavicharn, P.E – Basler Electric Company
Gerald Johnson, P.E – Basler Electric Company

I. Introduction

Differential protection is usually applied on bus protection because of its high selectivity since it does not need to coordinate with other relays. Bus differential protection in power system networks operates on a principle defined by Kirchoff's current law. The law states that the vector sum of all currents entering and leaving a node or bus is equal to zero. It is this principle that is used in all bus differential protection regardless of the relay type used.

Currents entering and leaving a bus are resolved by a relay through current transformers (CTs) which accurately recreate the primary bus current at a specified ratio up to the point of CT saturation. CT saturation can occur during faults external to the differentially protected zone. The resulting relay misoperation is a weakness in a bus differential protection. For proper operation, bus differential relays must be able to distinguish between true internal faults and false differential currents caused by CTs saturation.

The location of CTs defines the bus protection zone. A simple scheme of bus differential protection can be achieved by paralleling CTs from all of the circuit breakers on the bus. The sum of current on each phase is zero for normal through-load and external through-fault conditions.

This paper discusses the fundamentals of bus protection with a focus on the two common methods typically used: high-impedance and low-impedance bus differential relaying. Included are the basic theories of high-impedance and low-impedance differential relaying and their operational concepts. A comparison between the two methods which points out the benefits, drawbacks, concerns and considerations is also given. . The importance of current transformer selection and performance are considered in this paper as part of the consideration in bus differential protection scheme design.

II. Low-Impedance Bus Differential Relaying

The differential relay current inputs of the low-impedance bus differential relays have, as the name implies, low impedance to the flow of CT secondary current. This concept is similar to a transformer percentage restrained differential relay except that the bus differential relay does not need to provide phase angle compensation. The relay computes the vector-sum of the normalized currents from all CT inputs. When properly connected, a vector sum of zero indicates a system with no internal faults however in practice even when perfectly balanced, the sum of the currents will never be exactly zero because of small differences and errors between the CTs. Current from an internal fault will result in a vector sum which is not equal to zero and cause a relay operation.

In a differential circuit, through current or normal load current flow through CTs is referred to as a restraint (I_R) quantity and differential current is defined as an operate (I_{OP}) quantity. The ratio of operate to restraint

current is referred to as “slope” which is usually indicated as a percentage, hence the name percentage-restrained differential. The restraint and operate quantities interact so that at higher levels of restraint current (I_R), the operate current (I_{OP}) will have to increase proportionally to operate the relay.

The equations below summarize the principal of restraint and operate currents [3].

$$I_{OP} = I_{DIFF} = |I_1 + I_2 + \ldots + I_n| \quad (1)$$

$$I_R = f(|I_1|, |I_2|, \ldots, |I_n|) \quad (2)$$

Various definitions of restraint current are being used in microprocessor-based relays. Examples are [3]:

$$I_R = \frac{1}{n}(|I_1| + |I_2| + \ldots + |I_n|) \quad (3)$$

$$I_R = \max(|I_1|, |I_2|, \ldots, |I_n|) \quad (4)$$

$$I_R = \frac{1}{2}(|I_1| + |I_2| + \ldots + |I_n|) \quad (5)$$

$$I_R = (|I_1| + |I_2| + \ldots + |I_n|) \quad (6)$$

Figure 1 shows the percentage current differential characteristic with dual slopes. Each characteristic provides a threshold (pickup) setting and at least one percentage restraint slope. The relay operates when I_{OP} is above a minimum threshold and is a percentage of I_R.

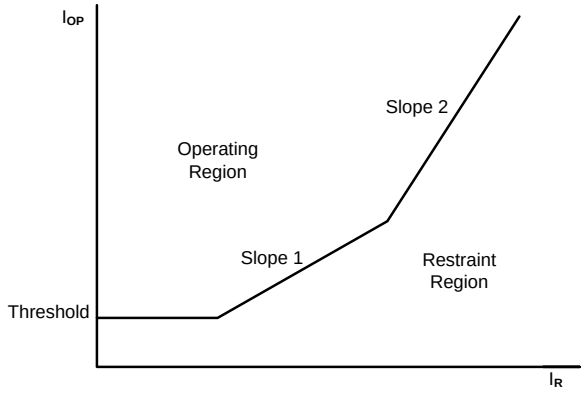

Figure 1: Percentage current differential characteristics with dual slope

Some installations use a transformer percentage restrained differential relay for a bus differential application. However, in the bus application the relay may be simpler as the CT tap adjustment and the harmonic restraint may not exist. The restraint slope may be fixed instead of being adjustable.

A. Multi-Restraint Bus Differential

The most involved version of this multi-restraint bus differential has all CT signals brought into separate restraint windings of the relay before being summed together by the relay for the operate circuit as shown below in Figure 2. Having individual CT signals allows the circuits to have different CT ratios. The relay uses individual tap adjustments to compensate for the difference in secondary current magnitudes which result from using CTs with different ratios.

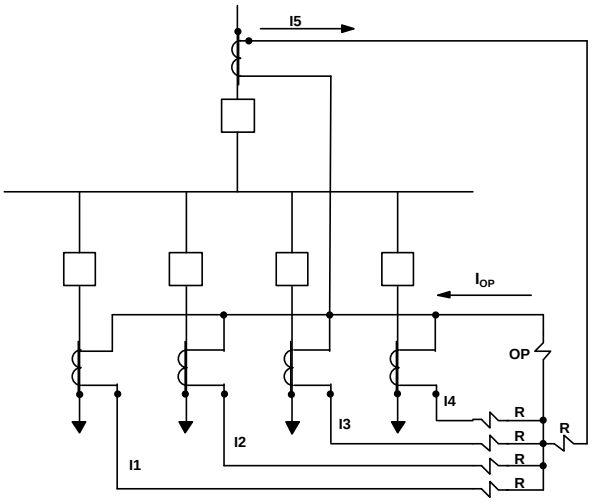

Figure 2: Multi-restraint bus differential schematic

Sometimes, two or more sets of CTs are paralleled and brought into one restraint winding of the relay. Paralleling CTs is possible by observing a few rules:

- Paralleled CTs must have the same ratio [9].
- Only CTs on the load side can be paralleled with minimal risk. Paralleling CTs on circuits with external sources of fault current increases the risk of CT saturation and therefore unwanted relay operation for a through-fault condition.
- The combined maximum load current from the paralleled CTs must not exceed the continuous rating of the relay current inputs [9].

CT polarity plays a critical role in proper current summation. Microprocessor-based low-impedance bus differential relays typically provide a means to change CT polarity sensing in the relay settings without rewiring CT inputs on the relay or changing CT polarity connection.

CTs should be chosen so that the AC voltage ratings are greater than the steady state AC voltage that will be seen by the CTs during an external fault. The greater the margin that is used, the less likely that transient DC induced saturation will occur.

One disadvantage of a low-impedance multi-restraint bus differential relaying can be the total number of restraint windings, which may limit future bus expansion. Application may also be prevented on buses with numbers of fault current source breakers exceeding the relay current inputs. In this case, the relay will require a restraint current input for each breaker in the zone.

One possible approach to setting the minimum sensitivity of a low-impedance differential relay is to select a minimum fault for which the relay should operate. It could be a value well below the minimum bus fault duty so that the relay operates quickly for a bus fault but is not set so low that a false operation could occur from through current. The other possible approach is to set the threshold (pickup) above the maximum current leaking from the differential zone. If there is a device that shows an inrush behavior or draws a steady charging current, the threshold setting should account for these values. If CT trouble conditions are of concern and no CT trouble monitoring function is available, the threshold setting could be set above the maximum load level.

A relay with a dual-slope characteristic as shown in Figure 1 requires a breakpoint value. The breakpoint should be selected to specify meaningful applicability of the lower (Slope 1) and higher (Slop 2) slopes. Slope 1 should be set to override false differential current caused by CT ratio mismatch, minor CT saturation, and transformer inrush currents however, it should provide sufficient sensitivity to detect internal bus faults. As the CT ratio errors cancel mutually to some extent, a setting of

10-25% of the maximum bus current is typically sufficient [3]. The breakpoint should be set below the current level at which the weakest of the CTs begins to saturate, including conditions such as DC offset or remnant flux, if the Slope 1 is set sensitively and accounts for only CT ratio errors. Slope 2 should be set to restrain false differential current caused by CT saturation during heavy external faults yet still be able to detect internal faults.

The formula for calculating the slope and for relay operation is:

$$I_{OP,pu} \geq I_R * \text{Slope} \qquad (7)$$

The required operate current will be higher for through-fault conditions. Note that restraint current calculations are manufacturer specific, refer to Equations (3 to 6).

Transformer differential relays are sometimes used for this type of bus protection. This type of relay does not differentiate well between an internal fault and an absolute and complete saturation of a CT during an external fault. The complete saturation of a CT during an external fault looks identical to an internal fault. For these relays to be secured against operation during an external fault there must be some assumption made of CT performance for an external fault. There are three approaches to prevent misoperation:

- Intentionally delay the relay operation so that it can ride through transient DC induced saturation.
- Use high performance CTs that minimize DC induced saturation.
- Set the relay to restrain for a lower level of CT saturation.

Depending on the manufacturer, transformer differential relays are characterized by restraint of operation if substantial 2nd or 5th harmonic currents are detected in the operate circuit. These features are intended to detect transformer inrush current and over-excitation of the transformer respectively. They may also be used to detect CT saturation in a bus differential protection scheme. A saturating CT will produce a reduced fundamental current with notable harmonic content. By setting the harmonic restraint so that a low level of harmonic current will block operation, it is possible to reduce the risk of relay operation due to CT saturation.

If harmonic restraint is used, it is important that no AC saturation should occur during an internal fault because the harmonic restraint may prevent relay operation during an internal fault if AC saturation occurs.

B. Unrestrained Differential

If the maximum possible false differential current is known, the relay may be set to initiate tripping regardless of the amount of the restraint current. This method is referred to as an unstrained differential, shown in Figure 3. It provides high-speed tripping for high level faults inside the protection zone.

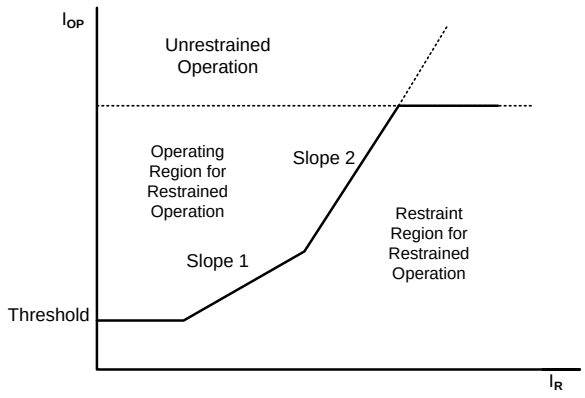

Figure 3: Percentage current differential characteristics with unrestrained operation

Typical settings of the unstrained element are in the range of 5-10 times CT nominal current and mostly depend on performance of the

CTs (class and burden) and external fault levels [3].

III. High-Impedance Bus Differential Relaying

A High-impedance bus differential relay includes high impedance to the flow of CT secondary current. The basic concept of this type of relaying involves taking the paralleled output of all CTs in the system and connecting them to a common bus which is then wired to the high-impedance bus differential relay as shown in Figure 4. Ideally, the paralleled CTs must have the same full ratio, have their secondary wound on a toroidal core with the winding fully distributed about the core (bushing type CTs), and have the same accuracy class. Proper polarity connection is also required to ensure that the secondary current outputs vector-sum to zero the same way the primary currents in the bus do under normal through-load conditions. The summation point for the CTs is frequently made in a junction box located in a switchyard with equal distance from each breaker to minimize the effect of unequal lead resistance. The summation point of each phase is then brought to the control house and connected to the relay. The relay operates based on the rising voltage which appears at the summing point when differential current flows through the high-impedance operate circuit.

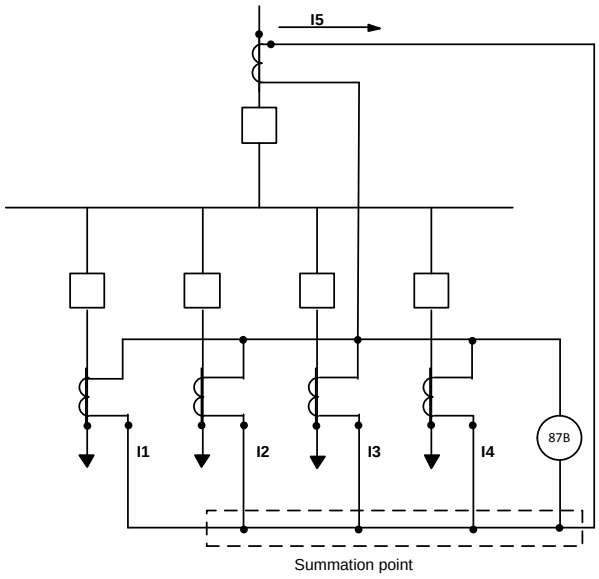

Figure 4: High-impedance bus differential schematic

The high-impedance input of the relay generally has an internal impedance of 1000 ohms or higher, depending on manufacturer, that is typically resistive. For non-fault conditions, the currents are balanced sufficiently so that the voltage across the relay's impedance is near zero. The weakest CT, fully saturated for an external fault, with all other CTs operating normally should be calculated to establish the starting point for the internal fault trip setting. This process is followed to prevent unwanted operation for an external fault. For an internal fault, all CTs try to force the differential current through the high-impedance input, creating the voltage drop used to trip for the internal fault condition. At this point, the voltage which appears across the relay is essentially the open-circuit voltage of the CTs. The resultant high voltage is the signature for fault detection. High-impedance differential relays typically have a means to control this high voltage to prevent CT, cable, and relay insulation breakdown. The two main methods for controlling this high voltage are non-linear impedances such as a Metal-Oxide Varistor

(MOV), paralleling with stabilizing resistance, and a static switching device such as a Silicon Controlled Rectifier (SCR).

In the application of a high-impedance differential relay, contacts from an external lockout device (86) should be wired across the voltage protection components allowing the relay to continue operation as a conventional overcurrent relay and at the same time protect against exceeding the short time rating of the voltage protection components until the fault is cleared (see Figure 5).

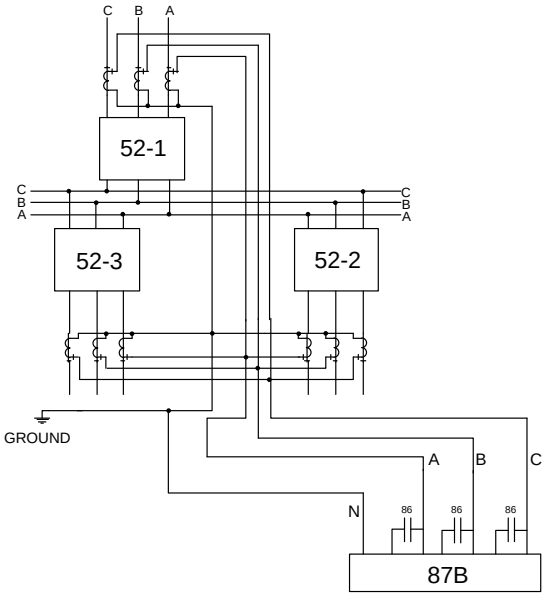

Figure 5: High-impedance bus differential relay connection

The trip setting on the high-impedance bus differential relay is set based on the voltage developed across the relay. The relay voltage threshold must be set above, with margin, the maximum possible voltage developed across the high-impedance input for an external fault. If a mixture of multi-ratio CTs is used (though not recommended) or if the CTs are applied on taps other than a full ratio, calculations must be performed to determine if excessive voltages will be produced across the full winding of the CT.

The minimum acceptable voltage threshold can be determined using the following equation.

$$V_{threshold} = \frac{I_F}{N} * (R_{CT} + R_L * P) \qquad (8)$$

Where:

I_F = the maximum fault current

N = CT ratio

R_{CT} = dc resistance of CT secondary winding and lead resistance up to the CT terminals (at maximum expected operating temperature)

R_L = a one-way dc resistance of a lead from the differential junction point to the fault CT terminals (at maximum expected operating temperature)

P = 1.0 for three-phase faults and 2.0 for single-phase-to-ground faults

Normally, the voltage $V_{threshold}$ is multiplied by a safety factor of 1.25 or higher for worst-case external faults. Therefore, the relay voltage setting should be:

$$V_{relay} = K * V_{threshold} \qquad (9)$$

Where:

K = margin for safety to ensure secured operation, usually 1.25 or higher

The following may be observed with respect to evaluation of Equation (8).

- It is only necessary to calculate three-phase and single-phase-to-ground faults. If the results yield a satisfactory application, the application will also be satisfactory for multiple-phase faults.
- For single-phase-to-ground faults, the relay differential circuit is such that the

CT secondary fault current will flow through both of the fault CT leads. Therefore, the multiplier P must be equal to two. Conversely, the CT secondary currents during a balance three-phase fault will result in zero current in the return lead. Therefore, only one-way lead resistance is involved and P is equal to one.

- If the single-phase-to-ground fault current at a given location is greater than or equal to the three-phase fault current, the calculations need only be performed for the single-phase-to-ground faults.
- The resistance of the CTs and leads will increase as the temperature rises. If adequate margin is to be maintained at all times, Equation (8) should be evaluated using resistance values corresponding to the maximum expected operating temperature.

For bus protection applications, the following two methods, using Equation (8) and Equation (9), may be used to determine the appropriate relay voltage setting.

1. Method 1: Simplified Conservative Approach

With this method, it is assumed that a single-phase-to-ground fault with a current magnitude equal to the maximum interrupting rating of the breaker occurs on the feeder associated with the CT having the longest lead run from the differential junction point. Under this assumption, the effect of the fault current I_F is maximized and so is the effect of lead resistance because the highest value of resistance is used. P is set equal to two. Therefore, the maximum possible value of $V_{threshold}$ will be obtained. The following delineates the requirements to calculate the relay settings.

a. Use the maximum interrupting rating of the circuit breaker as the maximum single-phase-to-ground fault current (I_F).
b. R_L is based on the distance from the differential junction point to the most distant CT.
c. Calculate $V_{threshold}$ substituting the values of current and resistance from a. and b. and set P = 2.0.
d. Substitute $V_{threshold}$ from c. in Equation (3) to determine the appropriate relay voltage setting.

2. Method 2: Exact Approach

With this method, calculations must be performed for the maximum single-phase-to-ground fault and the maximum three-phase fault of each of the n feeders on the bus. Therefore, Equation (8) must be evaluated 2n times using the associated value of lead resistance and P = 1.0 or P = 2.0. The following defines the process for developing the setting.

a. Determine the maximum three-phase and single-phase-to-ground fault currents for faults of each of the n breakers on the bus.
b. R_L is the one-way dc resistance of the lead from the associated CT to the differential junction point.
c. Calculate $V_{threshold}$ separately for each breaker, utilizing the associated maximum external three-phase symmetrical fault current in the fault CT with P = 1.0 and the maximum external single-phase-to-ground fault current in the fault CT with P = 2.0.
d. Use the highest $V_{threshold}$ resulting from the calculations in c.
e. Substitute $V_{threshold}$ from d. in Equation (9) to determine the appropriate relay voltage setting.

In general, Method 2 will produce a lower relay voltage setting than Method 1. Method 1 is simpler to use and therefore should be employed first. If the resultant relay voltage setting from Method 1 is adequately sensitive then there is a unique advantage in that the setting does not require recalculation following future changes in the power system that result in higher fault current magnitudes. Method 2 should be used if the result of Method 1 does not prove to be adequately sensitive.

High-impedance bus differential relaying is a popular method for bus protection on high voltage and essential medium voltage buses. It also becomes more predominant on high fault duty switchgear where the enclosed space of the bus allows little room for dissipation of arc energy since it provides both high security for external faults and high sensitivity for internal faults. Very little difference current is required to generate a voltage drop across the high-impedance input to initiate a trip, and therefore, resulting in high sensitivity.

A. Mixing different ratios of CTs

There are applications which require that different CT ratios be mixed in a high-impedance bus differential protection scheme. The most common cause is when an existing breaker is replaced or upgraded. Sometimes the CT ratio of the new breaker cannot be matched to the old breaker because the current rating of the new breaker is considerably higher than the breaker it is replacing. Three methods that could be used to work with the mixed CT ratios are discussed below.

1. Using partial taps on CTs

This method has two difficulties:

- CT overload: Suppose there is a mix of 3000 A and 1200 A breakers on the same bus. Typically, a 1200 A breaker has 1200:5 multi-ratio (MR) CTs and a 3000 A breaker has 3000:5MR CTs. One solution to consider is to tap the 3000:5MR CTs at 1200:5. If 3000 A flows through the breaker, the 1200:5 tapped CTs will be carrying (3000/1200)*5 = 12.5 A secondary. This would mean that the CTs must have high thermal rating factor to carry this current otherwise the CTs will be overloaded, making this method unadvisable.
- High voltage across the open terminals of the CT: When an internal bus fault occurs, the voltage across the open winding tap will be higher than the relay setting by a factor determined by the CT turns ratio. Based on IEEE C57.13, the CT internal wiring should be insulated to 3500 V crest. One must be aware that any wiring between the CT and the relay might also see the peak voltage. If tapped CTs are going to be used on high-impedance bus differential schemes, it is prudent to consult with the CT manufacturer on the CT insulation ratings and to check all wiring and terminal block voltage ratings.

2. Connecting two CTs in parallel

This method could be used to effectively obtain a lower CT ratio. Figure 6 shows two 3000:5 CTs in parallel. This arrangement sums to a total current that is equivalent to a single 1500:5 CT. It is an effective method but requires the luxury of having two CTs.

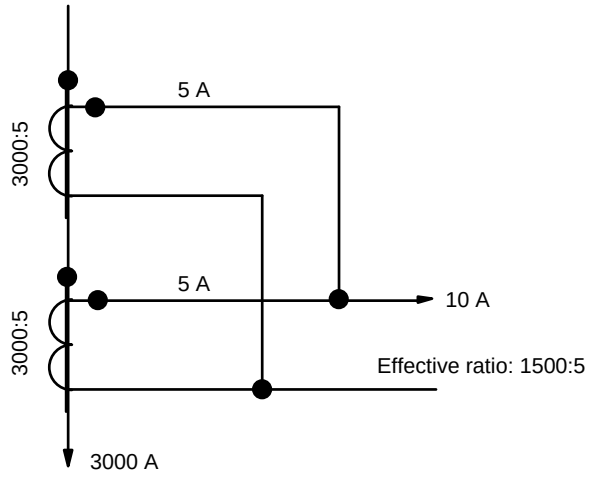

Figure 6: Paralleling two CTs

3. Interconnecting CTs at tap or Autotransformer

This method involves connecting lower ratio CTs to higher ratio CTs at an appropriate tap. This is then connected to the high-impedance bus differential relay across the full higher ratio tap (see Figure 7).

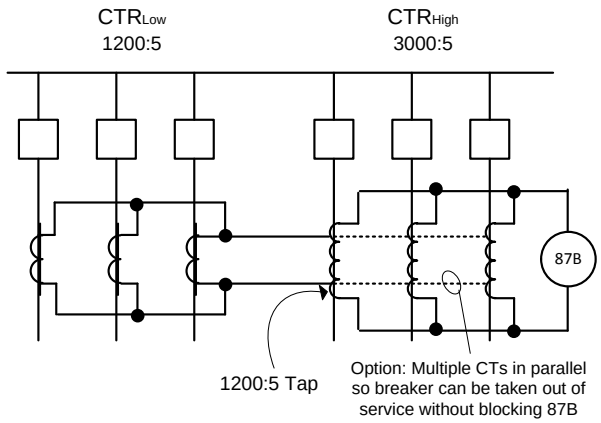

Figure 7: Paralleling different ratio CTs through tap connections

From Figure 7, the interconnection of the taps could also be extended to the other higher ratio CTs so that several higher ratio CTs are performing the transformation of the lower ratio CTs currents. This allows any one of the associated breakers to be removed from service without disabling the bus protection scheme.

When using this method, the engineer must consider the various operating contingencies to ensure that CTs will not be driven past their thermal rating factor.

IV. Concerns and Considerations

A. Current Transformer (CT) Performance Consideration

As mentioned before, CTs play a critical role in bus differential protection. Understanding the performance of CTs is critical to the analysis of a bus differential protection scheme. There are several reasons CT saturation becomes a concern for bus differential relaying more so than with other types of relaying. Some of these reasons are:

- The saturation tends to cause misoperation. Misoperation of a bus differential relay is likely a major problem.
- In some cases, high speed line relays make their tripping decisions within a cycle, before the effects of DC offset saturation come into full effect. .
- The effects of DC offset are short lived. Typical system X/R ratios are in the range of 3-15, yielding L/R time constants of 0.5-2.5 cycles on a 60 Hz base. After the DC offset passes, the CT starts to output more normal current waveforms. This allows the relays to make correct decisions again. The worst window of CT error due to saturation is likely less than 10 cycles.
- Saturation is rarely complete; a saturated CT still has some secondary voltage and current.

For an external fault, the CTs nearest the fault will see higher currents than other CTs in the

zone of protection. In radial single source systems, all of the source side CTs will also see the same fault current. Assuming all CTs are rated the same and have the same ratio, the CTs seeing the highest current are usually at the greatest risk of going into saturation. This is usually considered the worst case for which bus protection must be designed.

1. Steady state AC saturation

To determine if a CT is rated for an application, calculations must be performed to determine whether the AC voltage that will be impressed on its secondary during a fault will exceed the AC voltage that the CT can support. This is typically calculated using fundamental frequency values of AC current with no DC offset.

The voltage that the CT is rated to drive varies. There are three common approaches for determining the voltage:

- The IEEEC57.13 “knee point”: constructed using the intersection of the excitation curve and a 45˚ line as shown in Figure 8.
- The “saturation voltage”: using the intersection of straight lines drawn from the two sections of the curve as shown in Figure 8.
- The “C” rating of the CT: the C rating calls for less than 10% error in secondary current at 20 times rated current into 1, 2, 4, or 8 W 0.5pf burdens. This specifies that the CT shall be able to reproduce 100 V, 200 V, 400 V, or 800 V at its terminals with 100 A flowing into 0.5pf burden.

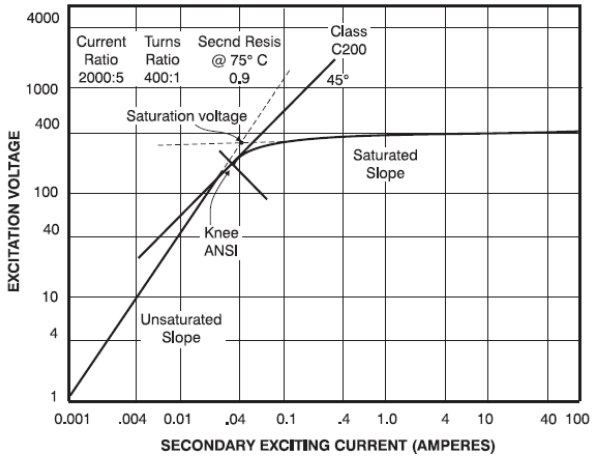

Figure 8: Typical CT excitation voltage versus excitation current curve

2. DC offset and residual flux induced saturation

The effect of the worst case DC offset, the worst case AC current, and the worst case residual flux in the CT will cause at least a small amount of transient CT saturation in a CT that is otherwise totally acceptable for steady state AC fault current. With either a higher fault current or CT secondary burden, a higher CT secondary voltage and a higher CT flux level will result. Figure 9 shows the flux buildup that will occur in a CT during an event, assuming a pure resistive secondary circuit and an infinitely permeable core.

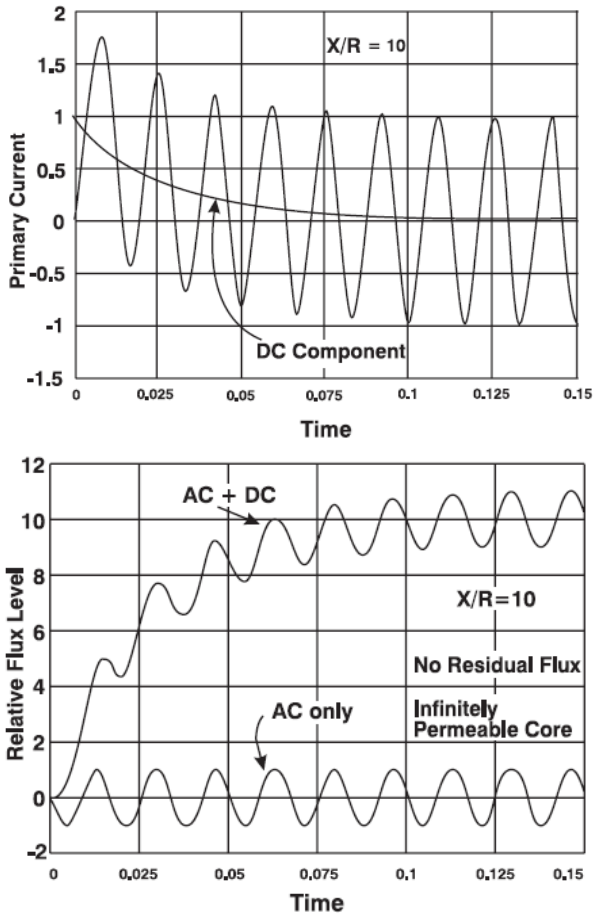

Figure 9: CT flux levels with DC current effects, infinitely permeable core

Figure 9 does not show any residual flux at the start of the process. In practice all magnetic cores hold some level of flux after current is removed. During normal operation, a CT reproduces an AC waveform for an indefinite period with core flux levels that are constantly offset from a zero flux level. The offset tends to be the worst immediately after a major reduction in current levels and tends to decrease with time. Based on IEEE C37.110 the residual flux level found in a variety of CTs varies over the range of 0-80% of design flux level. Residual flux may be oriented in either direction. Therefore, the flux indicated in Figure 8 may be shifted up or down depending on the level of residual flux.

Realistically core flux levels do not reach the levels shown in Figure 9. The core reaches a level of flux density and the flux levels do not appreciably increase after that point. Therefore, the CT output drops to zero until current flows in the negative direction to de-saturate the CT. As the DC offset decays, the CT output gradually improves until the secondary current represents the input waveform. In reality, for the primary current shown in Figure 9, the output waveform takes on the form shown in Figure 10, assuming a maximum relative flux level of 2. The waveform shown is a result of a resistive secondary burden. An inductive burden results in a decayed dropout of the secondary current. The resultant current has more of a sinusoidal waveform. The points to note for a bus differential scheme relating to CT saturation are as follow:

- Saturation may occur very quickly, as fast as the first half wave of the primary current wave. This needs to be accounted for in the setup of a bus differential scheme.
- In a saturated CT, as the primary current DC offset decays, the output waveform returns to a normal AC waveform.

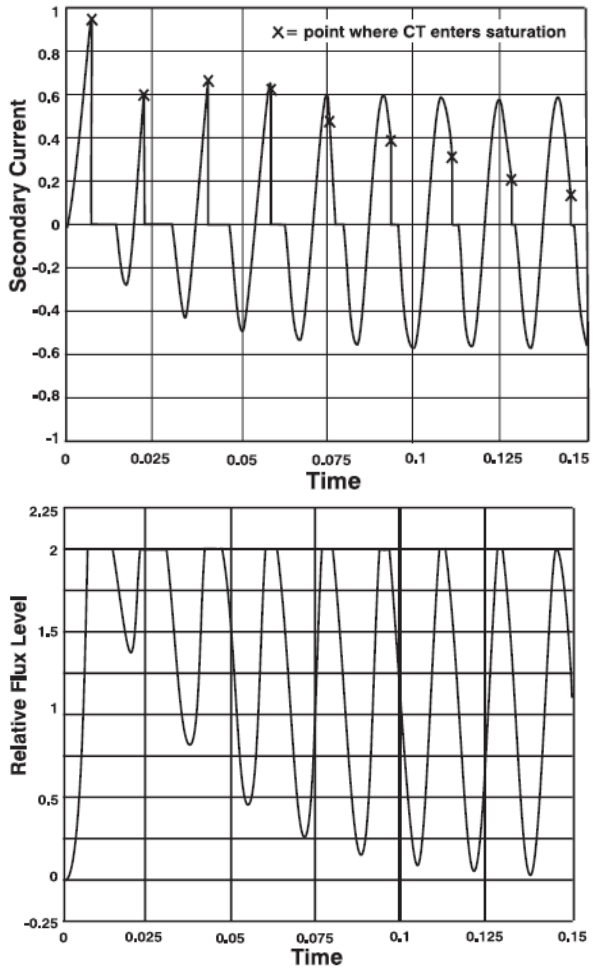

Figure 10: Saturation effects on an actual CT

In conclusion, to avoid saturation from the effects of DC offset (ignoring residual flux effects), a CT needs to be rated for a voltage that is 4-16 times the rating required for the steady state AC voltage. When considering the effect of residual flux, the allowance that must be made to avoid saturation may need to be even higher than 4-16 times.

The formula for calculating CT voltage to avoid the effects of DC offset is:

$$V_{CT,Rated} \geq K \left(1 + \frac{X_{L,p}}{Rp} \right) * I_{sec,rms} * R_{sec} \quad (10)$$

Where:

K = margin/safety factor to account for uncertainties such as the effects of residual flux and circuit modeling error

$X_{L,p}$ = CT primary circuit inductance

R_p = CT primary circuit resistance

$I_{sec,\ rms}$ = secondary current in rms

R_{sec} = CT secondary circuit resistance

C. CT Performance Requirements for Low-Impedance Bus Differential Relays

Generally, avoiding CT saturation for bus differential applications is preferable. In reality, completely avoiding CT saturation is virtually impossible. Therefore, the low-impedance bus differential relays must tolerate some degree of CT saturation. CTs should be chosen to have an AC voltage rating higher than the steady state AC voltage seen by the CTs during an external fault.

CT saturation is quite common in industrial switchgear applications. Often, the switchgear contains relatively low-ratio and low-accuracy CTs because of their lighter weight, smaller size, and lower cost than higher-accuracy and higher-ratio CTs. The combination of low-ratio and low-accuracy ratings increase the likelihood of CT saturation as fault current levels and source X/R ratios increase [9].

Low-impedance bus differential relays employ different techniques to help lessen the effects of CT saturation during external faults that otherwise would result in misoperations. A percentage current differential characteristic, as shown in Figure 1, is commonly used in low-impedance bus differential relays. Relays can have a fixed-slope, a single-slope, or a dual-slope characteristic. Relays with a dual-

slope characteristic greatly mitigate the effects of CT saturation at higher fault currents.

Multi-ratio CTs used in bus differential protection should be connected so they are at their maximum ratio for the best performance during fault conditions. Individual CT inputs on low-impedance bus differential relays have a tap adjustment or a magnitude compensation setting necessary to normalize currents from different CT ratios. Relays typically limit the tap adjustment range. This, in turn, limits the range of CT ratios that the relays can accommodate.

In some installations, especially in distribution substations, CTs are summed together rather than bringing each CT into an individual restraint winding of a relay, as shown in Figure 11. When employing this practice, an engineer must be aware that paralleling CTs presents a possibility that a relay may see no restraint current. For the external fault shown in Figure 11, the current path indicated as I_1 represents a large through-current. If there was a source on one of the adjacent feeders or if a bus tie is feeding the bus, as indicated by current path I_2, the relay sees only the CT error and no through-current restraint. This will result in the relay having a greater tendency to operate for CT saturation. To avoid this condition, the Tie breaker CT should be put on a separate restraint winding if possible.

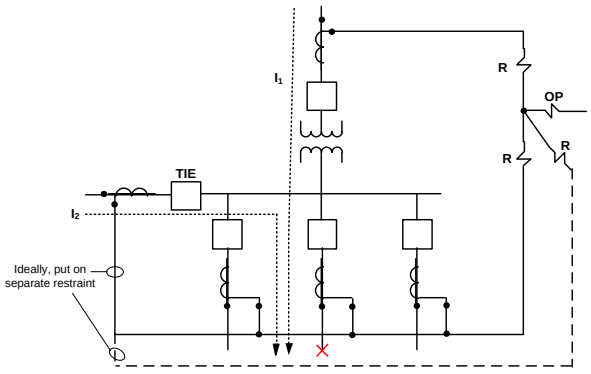

Figure 11: Multi-restraint bus differential with paralleling CTs

D. CT Performance Requirements for High-Impedance Bus Differential Relays

The possibility of CT saturation becomes a major concern in high-impedance bus differential relays because of their speed and the sensitivity they have to CT error. To secure operation of high-impedance bus differential relays for external faults, the relay tripping threshold voltage needs to be set appropriately.

CTs with higher accuracy class and ratios are strongly recommended for high-impedance bus differential relays. CTs with higher ratios reduce the secondary CT circuit voltage developed for an external fault. However, this benefit is almost offset by the higher internal CT resistance associated with a higher number of turns. CTs with a higher accuracy class have higher internal CT resistance because of their larger core area and winding length. Despite these facts, higher ratio and accuracy class CTs are still recommended in high-impedance bus differential schemes.

Mixing CTs with different ratios is strongly discouraged because of the complexities that may come from reduced CT accuracy that is proportional to the CT tap used. If CTs with different ratios must be used, some methods are already discussed in Section III: High-impedance bus differential relaying.

Predictable CTs performance is critical to the effective operation of high-impedance bus differential relays. Where practical, the following CTs guidelines should be considered.

- All CTs should be of toroidal design and be fully distributed around the core to have negligible leakage reactance.
- All CTs should have the same full ratio value and be connected to the full ratio taps.
- All CTs should have the same voltage rating, accuracy class, and thermal rating.
- The CTs should be dedicated to the differential application.
- When adding to an existing differential scheme, at least one set of CTs in the new breaker should be ordered with the same ratio and accuracy class as the differential CTs used in the existing scheme.
- CTs cannot have primary or secondary voltage limiting devices, as the resulting short-circuit could cause an unwanted operation of the differential.

V. Comparison and Conclusion

Table 1 provides a comparison between high- and low-impedance bus differential relays. This includes microprocessor-based and solid-state relays. It is provided to raise awareness of typical considerations required to design bus differential protection schemes. It is not intended to favor one method over the other. Engineers must evaluate the advantages and disadvantages of each type for their specific application and installation.

Table 1: Comparison of high- and low-impedance bus differential relaying

	Low-impedance	**High-impedance**
Multiple CT ratios	Yes	Strongly not recommended
Paralleling CTs	Plausible if paralleled CTs are of the same ratio and are load side CTs (refer to Low-Impedance Bus Differential Section)	Yes
Numbers of current inputs	Limited by relays current inputs	Not limited (however, careful consideration must be taken when connecting more than 10 current inputs)
Future expansion	Limited by relays current inputs	Not limited (however, careful consideration must be taken when connecting more than 10 current inputs)
CT polarity compensation	Yes	No
Security	Good	Good
Sensitivity	Good	Depending on settings
Speed	< 34 ms at 2 multiples of pickup < 27 ms at 4 multiples of pickup	< 6 ms

VI. References

1. 2008, “IEEE Standard Requirements for Instrument Transformers”, IEEE Power Engineering Society, Sponsored by the Transformers Committee, IEEE Std C57.13-2008.
2. 2007, “IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes”, IEEE Power Engineering Society, Sponsored by the Power System Relaying Committee, IEEE Std C37.110-2007.

3. 2009, “IEEE Guide for Protective Relay Applications to Power System Buses”, IEEE Power Engineering Society, Sponsored by the Substation Protection Subcommittee, IEEE Std C37.234-2009.
4. Blackburn, J. Lewis and Domin, 2007, “Protective Relaying Principles and Applications” Third Edition.
5. Grainger, John J. and Stevenson Jr., William D., 1994, “Power System Analysis” International Edition.
6. Basler Electric, 2005, “Bus Protective Relaying Methods and Application”.
7. Basler Electric, 2005, “Mixing Different Ratio CTs in High-Impedance Bus Protection Schemes” Application Notes. Publication Number PC-BUS01.
8. Basler Electric, 2012, “Instruction Manual for Bus Differential Relay BE1-87B”. Publication Number 9282300990.
9. Schweitzer Engineering Laboratories, Inc., “Considerations for Using High-Impedance and Low-Impedance Relays for Bus Differential Protection”.
10. GE Multilin, “CT Saturation in Industrial Applications – Analysis and Application Guidelines”. Publication Number GET-8501.
11. GE Multilin, “High-Impedance Differential Relaying”. Publication Number GER-3184.

If you have any questions or need additional information, please contact

Basler Electric Company

12570 State Route 143, Highland, Illinois U.S.A. 62249-1074
Tel +1 618.654.2341 Fax +1 618.654.2351
e-mail: **info@basler.com**

www.basler.com

No. 59 Heshun Road Loufeng District (N),
Suzhou Industrial Park, 215122, Suzhou, P.R.China
Tel +86(0)512 8227 2888 Fax +86(0)512 8227 2887
e-mail: chinainfo@basler.com

111 North Bridge Rd #15-06 Peninsula Plaza
Singapore 179098
Tel +65 68.44.6445 Fax +65 65.68.44.8902
e-mail: singaporeinfo@basler.com